



HART-APL-DEV HART to Ethernet-APL Development



Description:

Hardware and Software development services to add the new Ethernet Advanced Physical Layer (APL) interface to HART transmitters. Starting with the HM-APL-PCB as a baseline, the solution is customized to meet feature and board size requirements to easily add APL to existing HART transmitters.

Or, the APL functions of the HM-APL-PCB can be customized and HART functions removed, so a new APL based transmitter can be quickly developed.



HM-APL-PCB Baseline Design

Features and Benefits:

- Easily convert existing HART Transmitters to APL
- Or, quickly design "direct to APL" transmitters without HART
- HART-IP protocol support included
- Reduced time to market
- Lower development cost
- Concentrate on your instrument features, not APL!





Onetime NRE charge that includes:

- Schematics
- Parts lists
- Complete source code
- Engineering support

Specifications:

HART Specifications HART 4, HART 5, HART 6, HART 7,

HART Physical Layer Spec HCF SPEC-54

APL Specifications Ethernet-APL Power Test Specification v1.1

HCF TEST-008

FCG TT20008 v1.0

Maximum Power Draw Power for peripherals

540mW 135mW

Memory

512KB Flash

Components:

MK-1112, 11/28/2022

APL Interface Texas Instruments DP83TD510E
Microcontroller STM32F417 ARM Cortex M4

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